REV	Description	Date
V1.0	First Release	2017-1-12

AC7010/AC7020 Schematics

Page Number	Description
Page01	Cover Page
Page02	Block Diagram
Page03	Zynq-7000 JTAG & Bank0
Page04	Zynq-7000 MIO Config
Page05	Zynq-7000 Bank13-34-35
Page06	Zynq-7000 Bank502
Page07	Zynq-7000 Power
Page08	DDR3
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Page11	UART, SD
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Title: Zynq-7000 Cover Page

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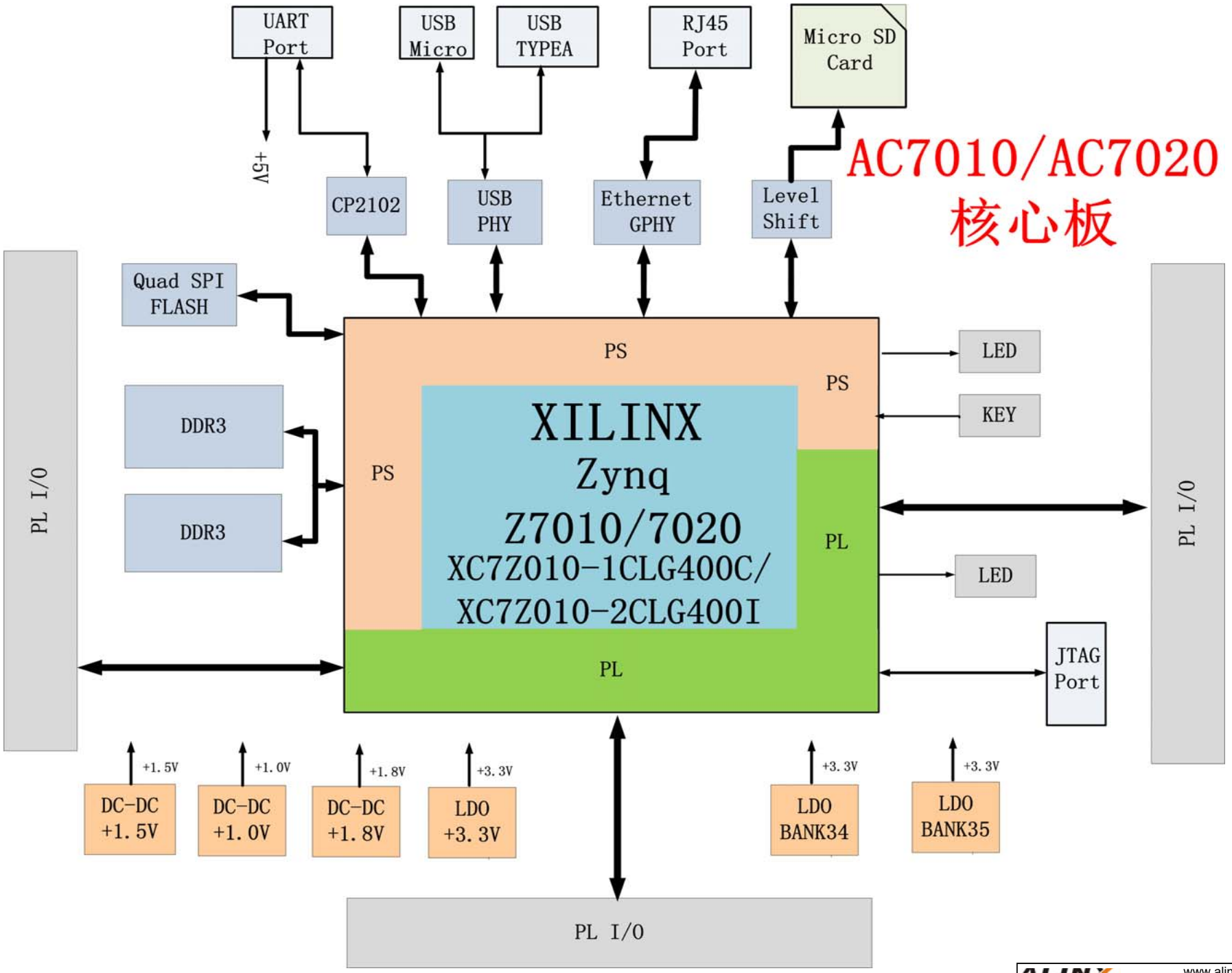

ALINX	www.alinx.com	
Title: Zynq-7000 Block diagram		
Size	Document Number: AC7010/AC7020 核心板Schematics	Rev: 1.0
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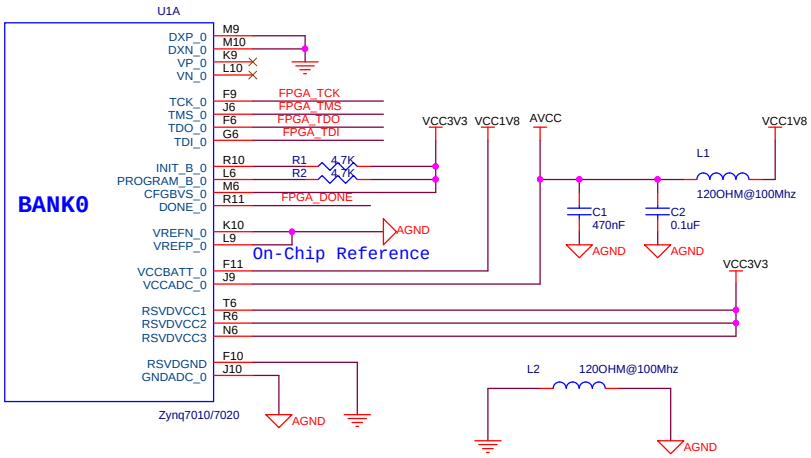
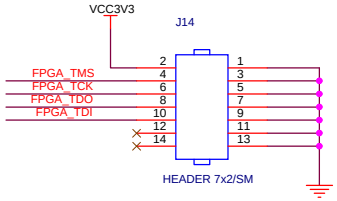
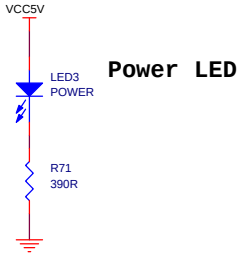
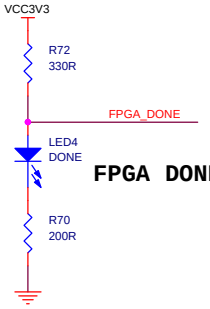




JTAG Connector



Power LED



FPGA DONE LED

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Title: Zynq-7000 JTAG & Bank0		
Size	Document Number: AC7010/AC7020 核心板Schematics	Rev: 1.0
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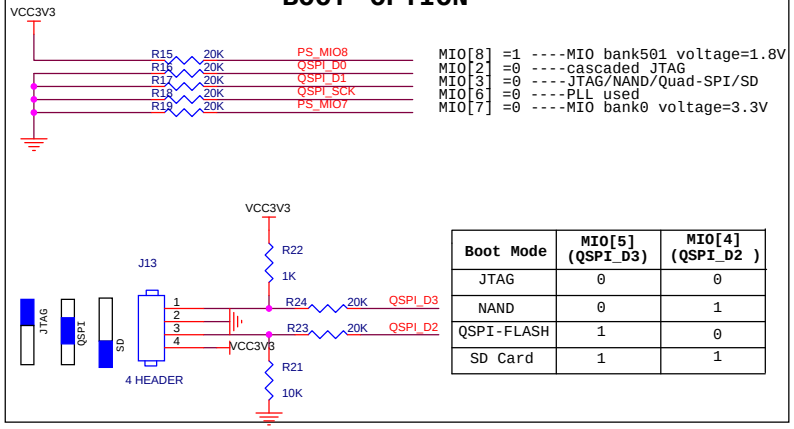
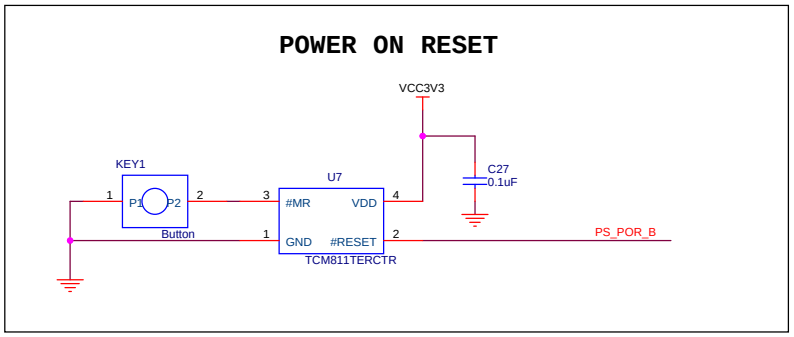
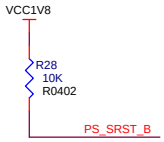
BOOT OPTION



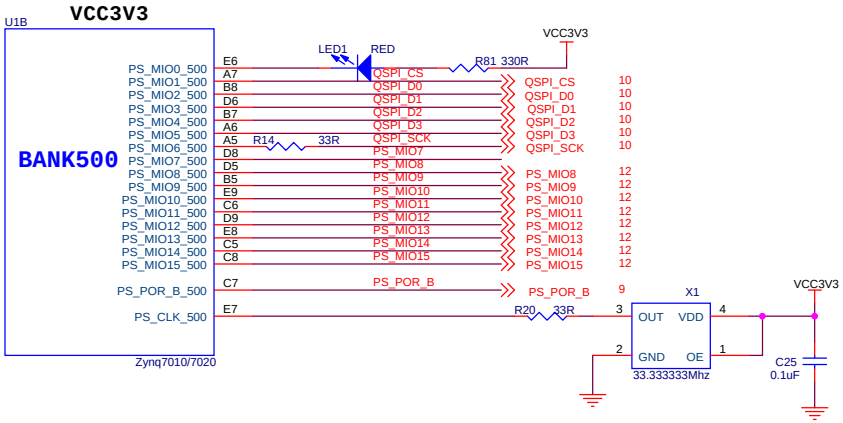
Boot Mode	MIO[5] (QSPI_D3)	MIO[4] (QSPI_D2)
JTAG	0	0
NAND	0	1
QSPI-FLASH	1	0
SD Card	1	1

POWER ON RESET

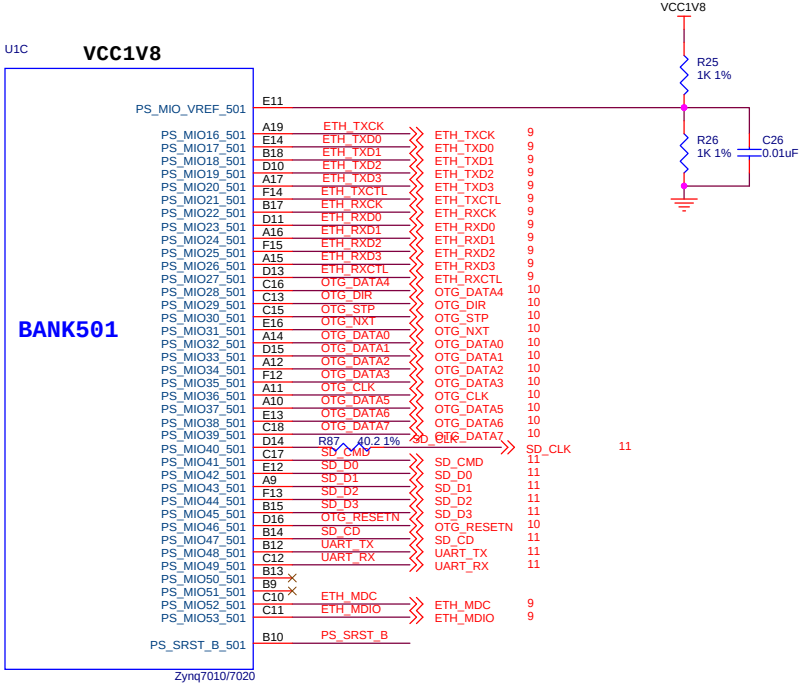




VCC3V3



VCC1V8



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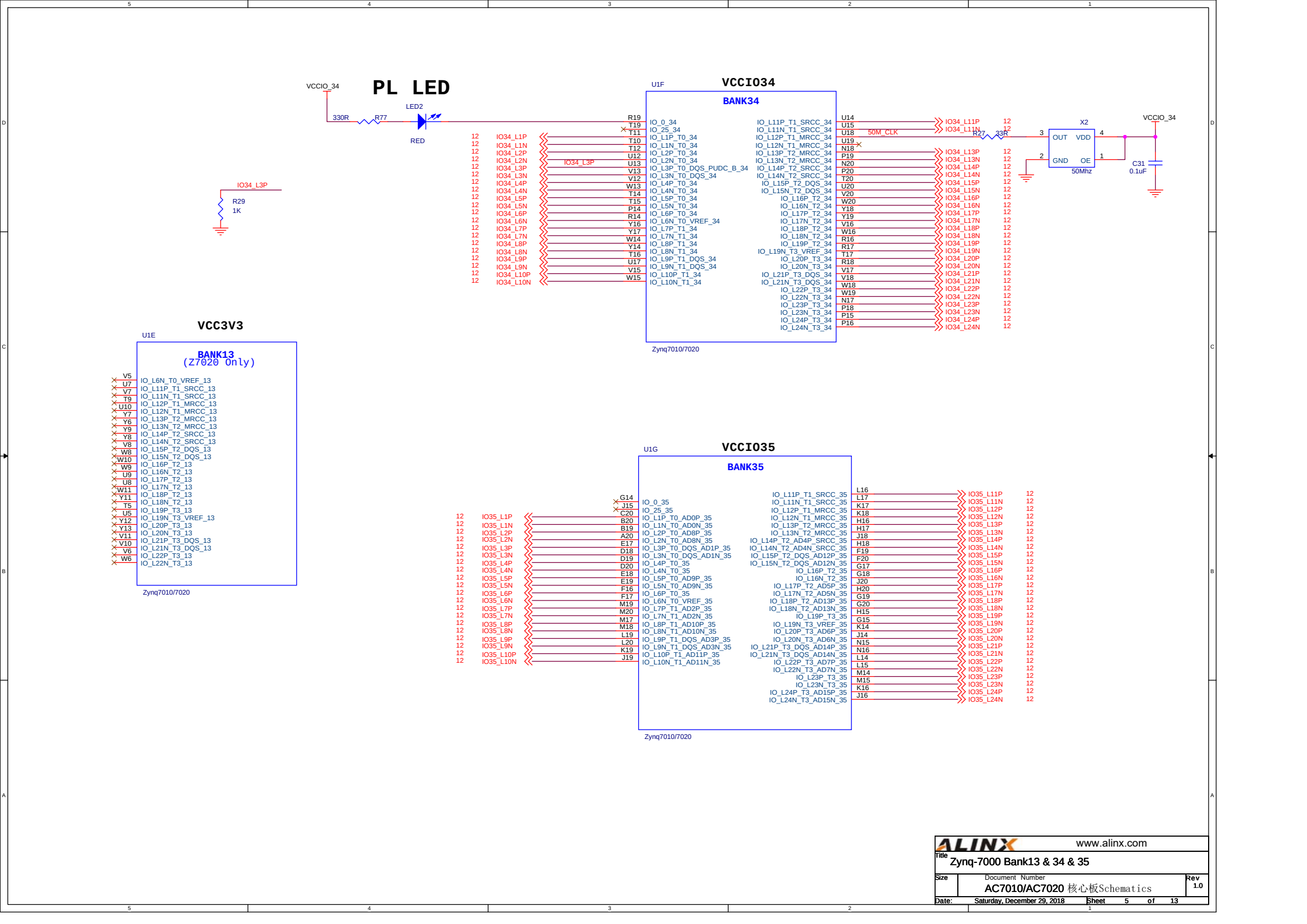
Title	Zynq-7000 PS MIO	
Size	Document Number: AC7010/AC7020 核心板Schematics	Rev 1.0
Date: Saturday, December 29, 2018	Sheet 4 of 13	


PL LED
VCCIO_34
330R
R77
LED2
RED
U1F
VCCIO34
BANK34
Zynq7010/7020
IO34_L3P
R29
1K
50M_CLK
R27
33R
X2
OUT
VDD
GND
OE
50Mhz
C31
0.1uF
VCC3V3
U1E
BANK13
(Z7020 Only)
U1G
VCCIO35
BANK35
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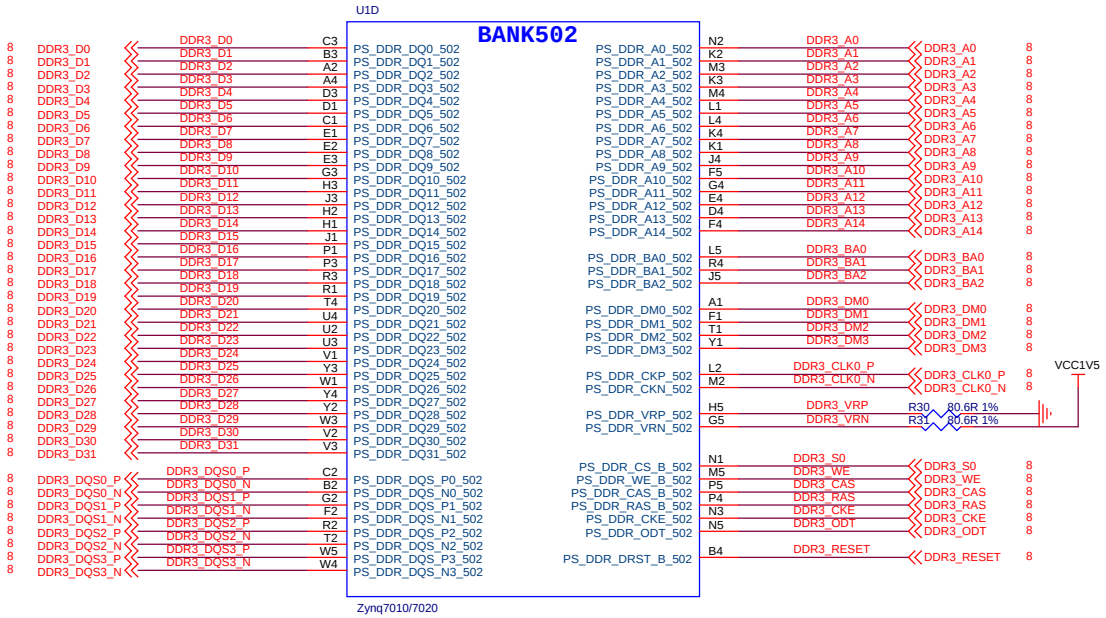
Zynq-7000 Bank13 & 34 & 35
AC7010/AC7020 核心板Schematics
Saturday, December 29, 2018



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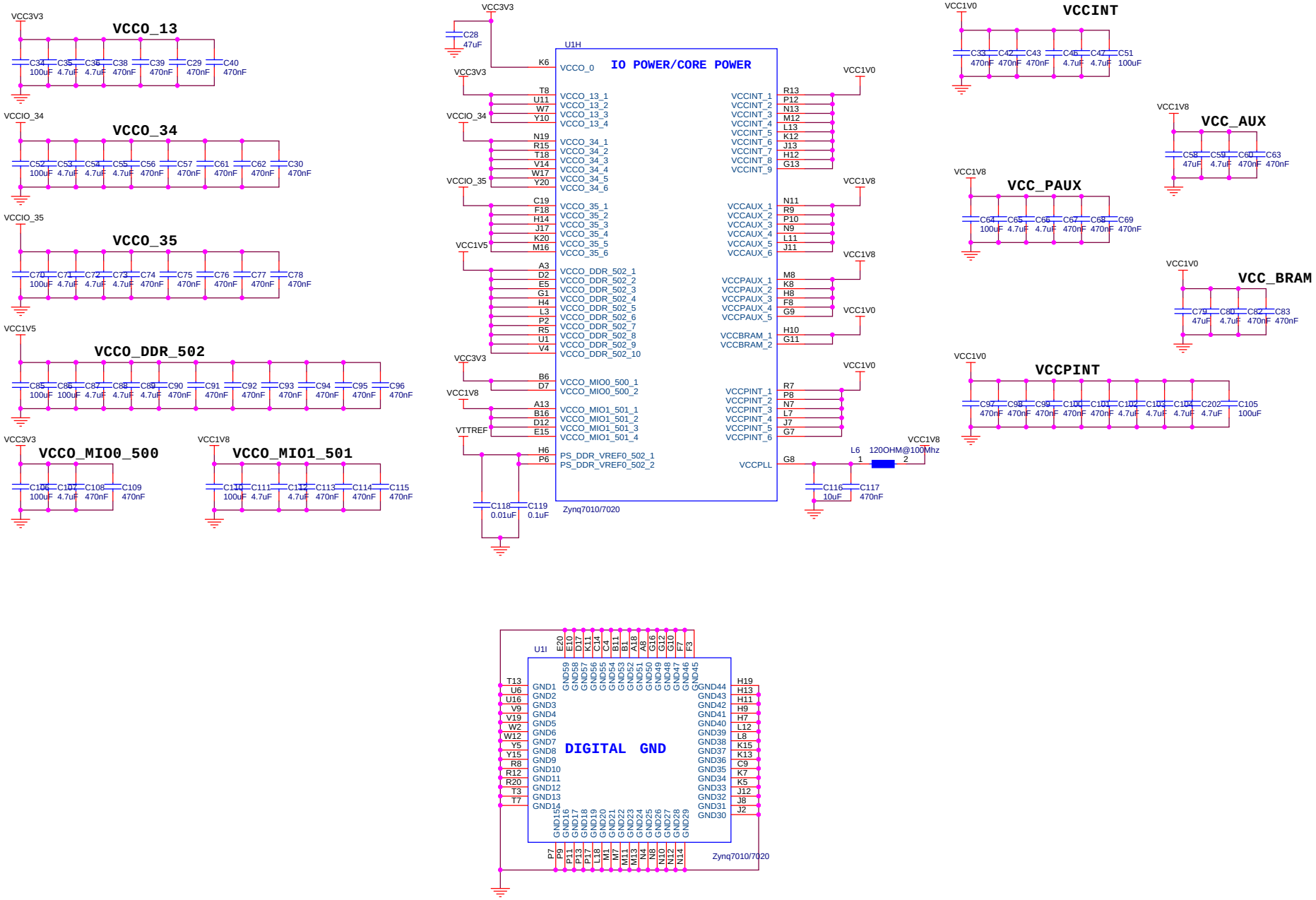
Title	Zynq-7000 Bank502	
Size	Document Number: AC7010/AC7020 核心板Schematics	Rev 1.0
Date: Saturday, December 29, 2018	Sheet 6 of 13	


VCCO_13
VCCO_34
VCCO_35
VCCO_DDR_502
VCCO_MIO0_500
VCCO_MIO1_501
U1H
IO POWER/CORE POWER
Zynq7010/7020
VCCINT
VCC_AUX
VCC_PAUX
VCC_BRAM
VCCPINT
U1I
DIGITAL GND
Zynq7010/7020
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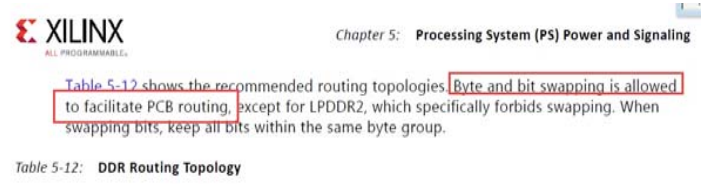
Saturday, December 29, 2018

为了 PCB 走线方便，DDR3 数据线组内（DQS除外 ）可以任意交换。XILINX的UG933文档的PAGE66有以下说明：



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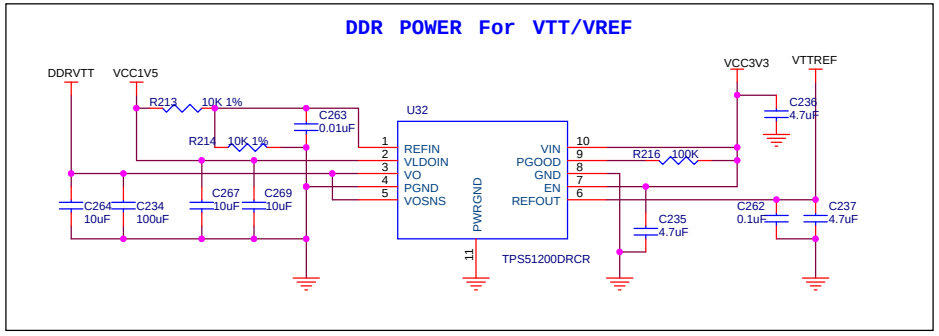
Chapter 5: Processing System (PS) Power and Signaling

Table 5-12 shows the recommended routing topologies. Byte and bit swapping is allowed to facilitate PCB routing, except for LPDDR2, which specifically forbids swapping. When swapping bits, keep all bits within the same byte group.

Table 5-12: DDR Routing Topology



Title	Zynq-7000 DDR
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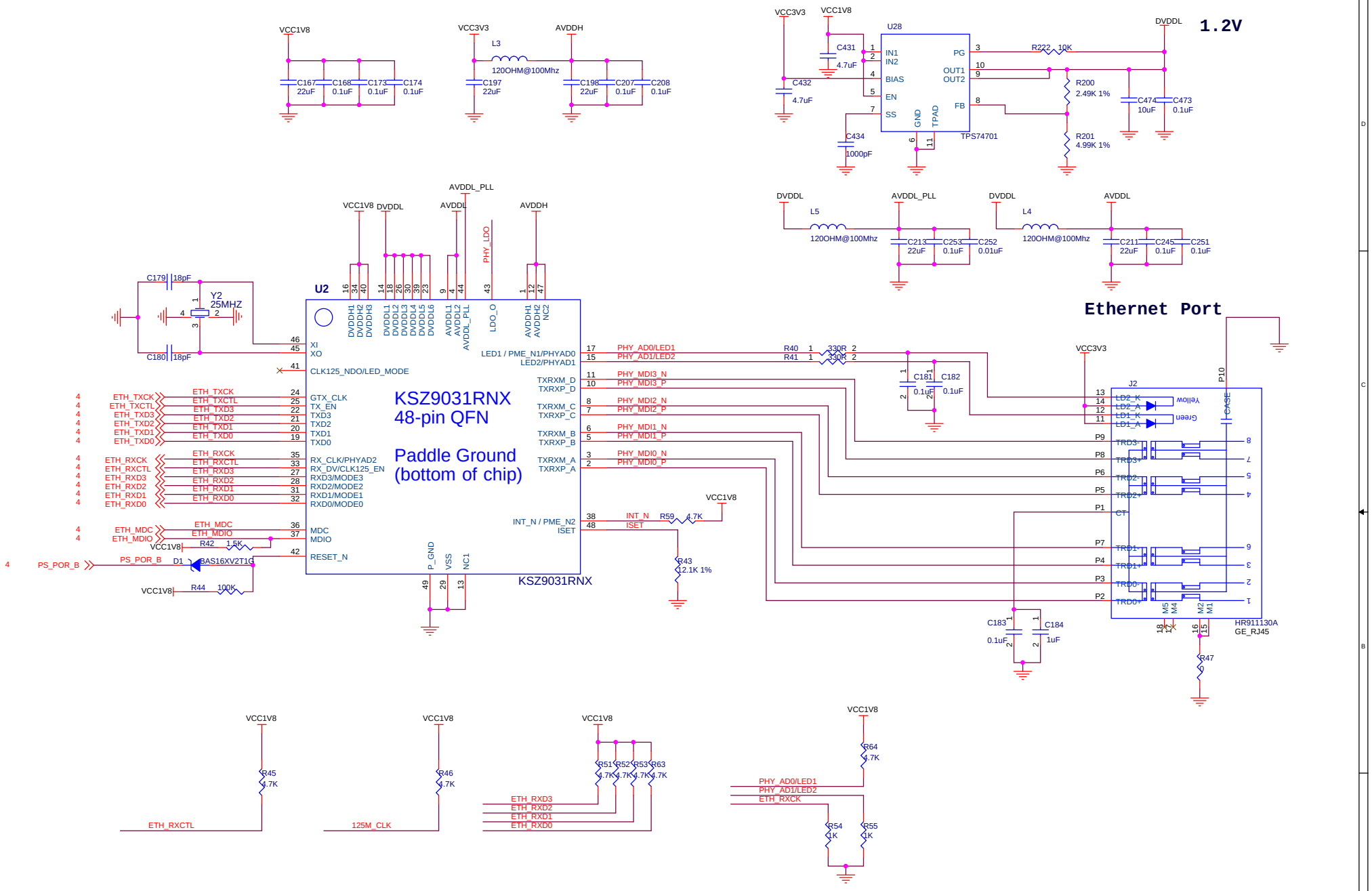
1.2V
Ethernet Port
KSZ9031RNX
48-pin QFN
Paddle Ground
(bottom of chip)
KSZ9031RNX
U2
U28
TPS74701
J2
HR911130A
GE_RJ45
Y2
25MHZ
Enable 125Mhz Clock out
Single-LED mode
RGMII mode - Advertise all capabilities
PHY Address is 001
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Zynq-7000 Gigibit PHY
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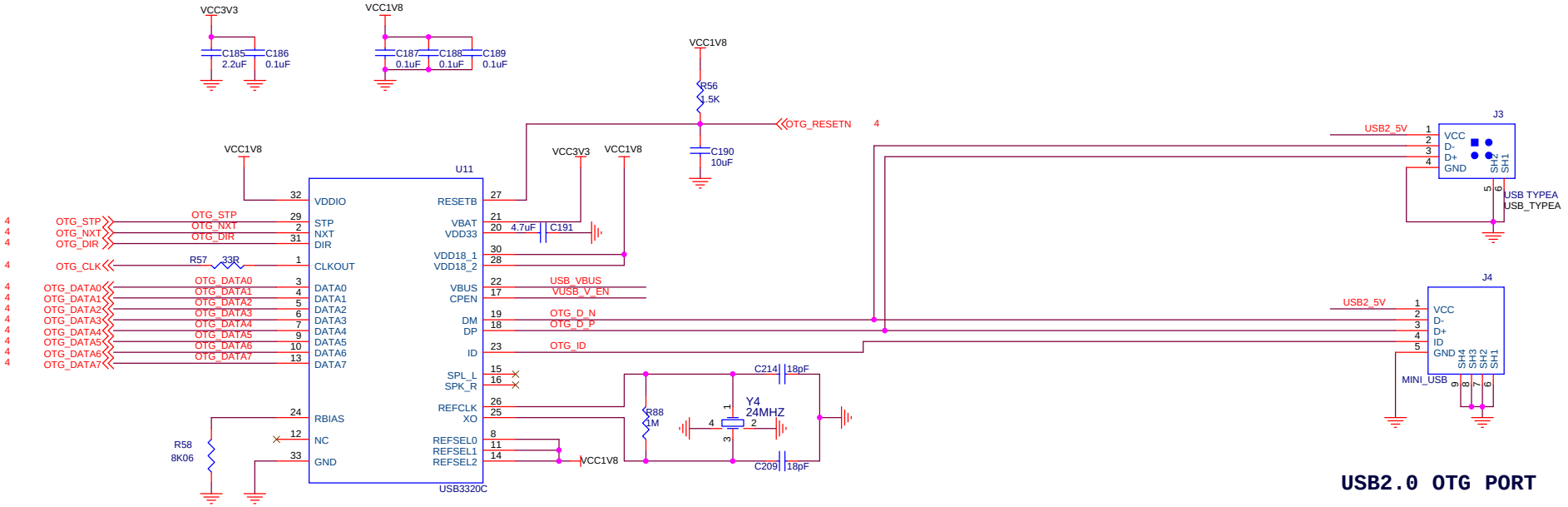
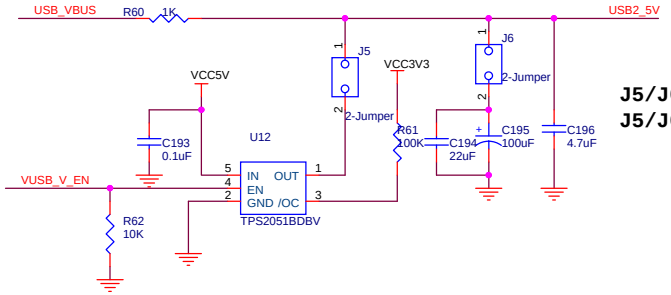
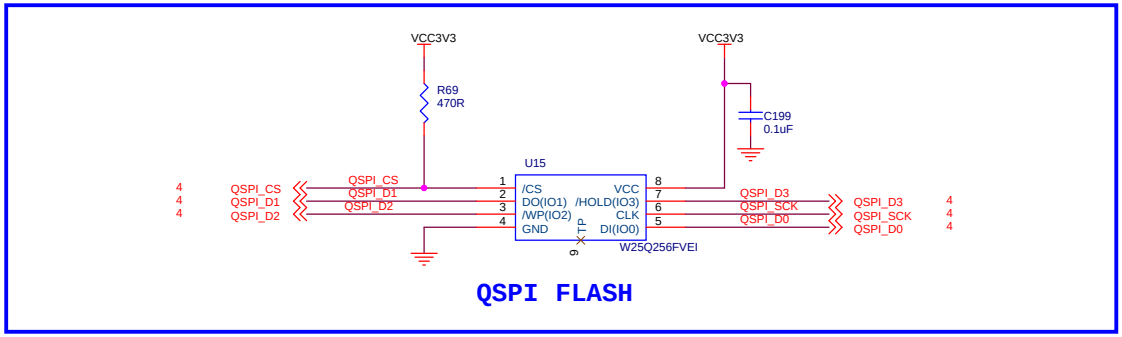
Wednesday, January 02, 2019



USB2.0 OTG PORT



J5/J6 Connect: Host Mode
J5/J6 Not Connect: Slave/OTG Mode



QSPI FLASH

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Title: Zynq-7000 OTG USB		
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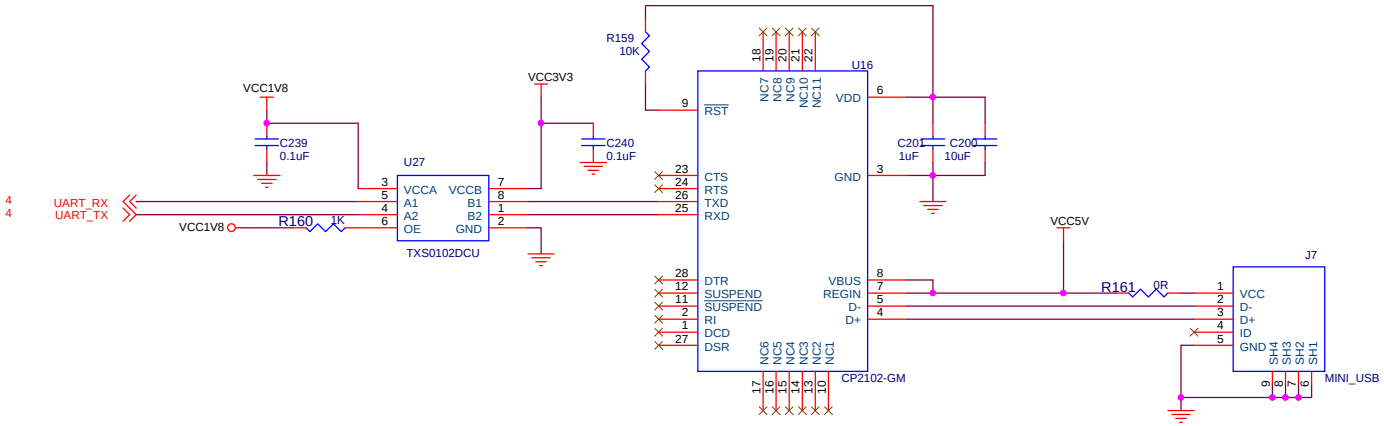
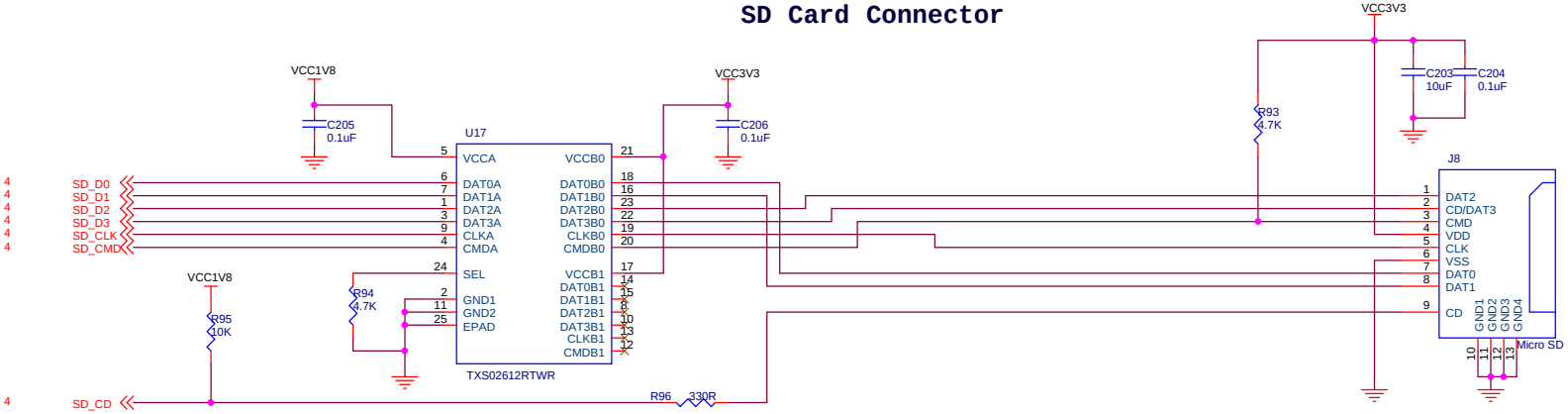
USB Uart



SD Card Connector



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Title: Zynq-7000 UART & SD		
Size	Document Number: AC7010/AC7020 核心板Schematics	Rev: 1.0
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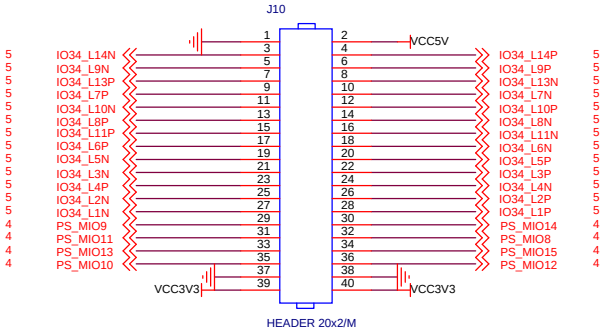
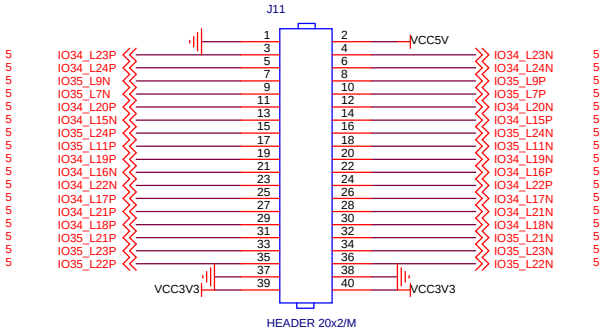
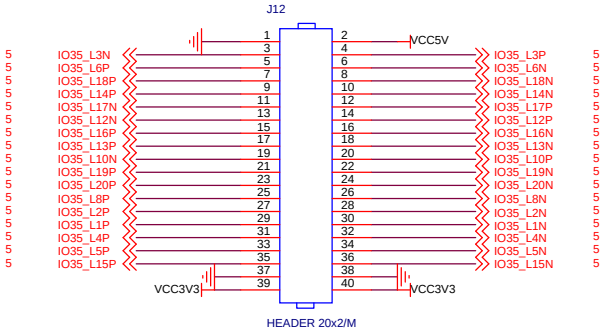
FPGA 40 PIN External IO







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Title: Zynq-7000 LED & KEY & IO

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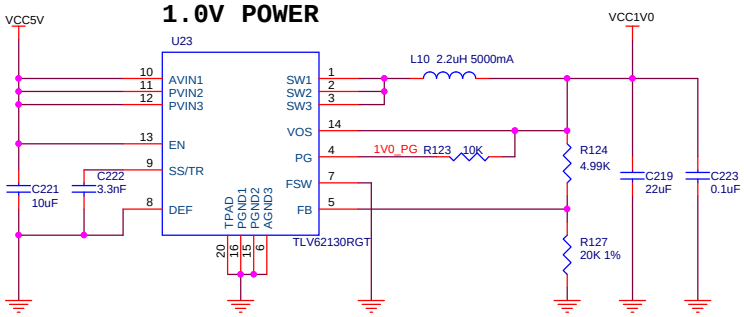

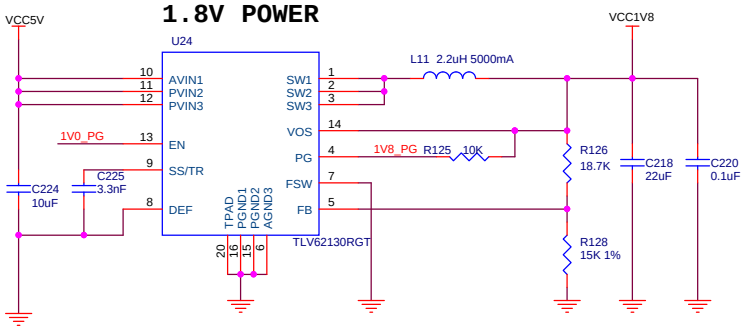

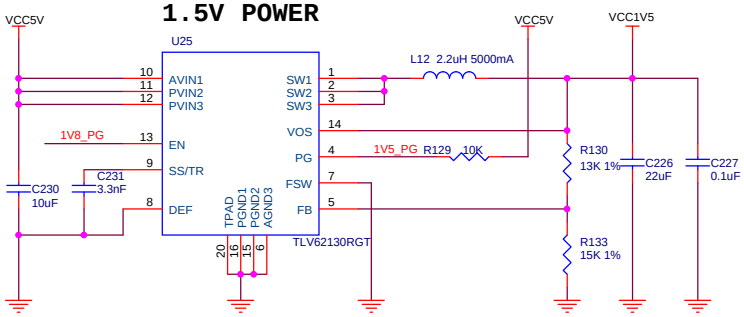

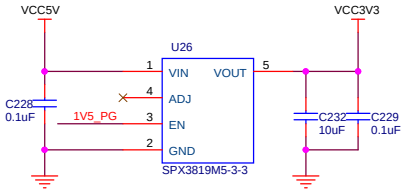

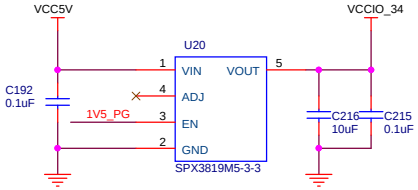

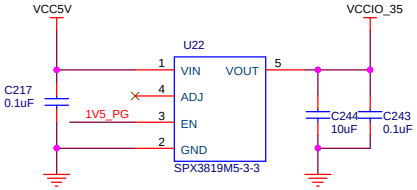

Power On Sequnce:

1.0V -> 1.8V -> 1.5 V -> 3.3V -> VCCIO

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Title: Power		
Size	Document Number: AC7010/AC7020 核心板Schematics	Rev: 1.0
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